This listing of claims will replace all prior versions, and listing, of claims in the application:

LISTING OF CLAIMS:

Claims 1-15 (Canceled).

Claim 16 (Currently Amended): A MOSFET device having a silicon substrate having shallow trench isolation STI, implanted wells, a gate dielectric, a deposited and patterned gate stack, implanted source/drain extensions, and a SiN etch stop layer deposited over the gate stack, the implanted wells and the implanted source/drain extensions, and an HDP oxide layer deposited primarily on horizontal surfaces over the SiN layer and over the gate stack, the implanted wells and the implanted source/drain extensions and used as protection from a fluorine implant to form fluorine doped low K dielectric oxide gate sidewall spacers, such that low-K properties of fluorine are used to develop a low parasitic capacitance MOSFET.

Claim 17 (Currently Amended): The MOSFET device of claim 16, having protection from a fluorine implant to form fluorine doped low K dielectric oxide gate sidewall spacers, and having a dielectric constant value in the range of 3.3 to 4.0.

Claim 18 (Currently Amended): The MOSFET device of claim 16, having protection from a fluorine implant to form fluorine doped low K dielectric oxide gate sidewall spacers, and having a dielectric constant value of substantially 3.3.

Claim 19 (Canceled).

Claim 20 (Currently Amended): The MOSFET device of claim 16, having protection from a fluorine implant to form fluorine doped low K dielectric oxide gate sidewall spacers, and further including a silicon nitride oxide layer formed over the MOSFET device.